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In the Claims

Please cancel Claims 8 and 9 without prejudice.

Please amend Claims 1 and 10.

PAGE 6/15 * RCVD AT 2/6/2006 4:23:39 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:12485404035 * DURATION (mm-ss):03-50

Listing of Claims

1. (currently amended) A stacked integrated circuit (IC) MIM capacitor structure comprising:

a first MIM capacitor structure disposed in a first IMD layer comprising a first upper electrode and a first lower electrode; and,

at least a second MIM capacitor structure arranged in stacked relationship in an overlying IMD layer comprising a second upper electrode and second lower electrode separate from said first upper and first lower electrodes to form an MIM capacitor stack;

wherein, the first lower electrode is arranged in common electrical signal communication comprising electrically communicating vias with the second upper electrode and the first upper electrode is arranged in common electrical signal communication with the second lower electrode to form said MIM capacitor stack in parallel electrical relationship-; and

wherein the respective upper and lower electrodes comprise a metal selected from the group consisting of Al, Cu, Ta, Ti, and nitrides that comprise silicided nitrides thereof.

2. (previously presented) The stacked MIM capacitor structure of claim 1, further comprising at least one additional MIM capacitor structure arranged in stacked relationship with

respect to an underlying MIM capacitor structure wherein respective upper and lower electrodes of respective odd and even numbered MIM capacitor structures in the MIM capacitor stack comprise a commonly communicating electrical interconnect structure in parallel electrical relationship.

3. (previously presented) The stacked MIM capacitor structure of claim 1, wherein the upper electrodes including electrically communicating vias of the respective MIM structures in the MIM capacitor stack comprise a substantially identical structure.

4. (previously presented) The stacked MIM capacitor structure of claim 1, wherein the lower electrodes including electrically communicating vias of the respective MIM structures in the MIM capacitor stack comprise a substantially identical structure in alternating IMD layers.

5. (previously presented) The stacked MIM capacitor structure of claim 1, further comprising a capacitor dielectric sandwiched between the respective upper and lower electrodes, said capacitor dielectric selected from the group consisting of SiO_2, Si_3N_4, TiO_2, Ta_2O_5, ZrO_2, Y_2O_3, La_2O_5, and HfO_2.

6. (previously presented) The stacked MIM capacitor structure of claim 1, wherein the electrically communicating vias comprise a metal selected from the group consisting of Al, Cu, W, and alloys thereof.

7. (previously presented) The stacked MIM capacitor structure of claim 1, wherein the

electrically communicating vias comprise a metal consisting essentially of W.

Claims 8-9 (cancelled)

10. (currently amended) A ~~The~~ stacked integrated circuit (IC) MIM capacitor structure of ~~claim 1, further~~ comprising:

a first MIM capacitor structure disposed in a first IMD layer comprising a first upper electrode and a first lower electrode;

at least a second MIM capacitor structure arranged in stacked relationship in an overlying IMD layer comprising a second upper electrode and second lower electrode separate from said first upper and first lower electrodes to form an MIM capacitor stack; and

bonding pads formed in electric signal communication with the uppermost MIM capacitor structure;

wherein, the first lower electrode is arranged in common electrical signal communication comprising electrically communicating vias with the second upper electrode and the first upper electrode is arranged in common electrical signal communication with the second lower electrode to form said MIM capacitor stack in parallel electrical relationship.

11. (previously presented) The stacked MIM capacitor structure of claim 1, wherein a lowermost MIM capacitor structure is formed in an IMD layer greater than about a second IMD layer formed over a semiconductor substrate.

Claims 12-21 cancelled

22. (previously presented) The stacked MIM capacitor structure of claim 1, wherein the first upper electrode is arranged in common electrical signal communication with the second lower electrode according to at least one second electrically communicating via extending through said first IMD.

23. (previously presented) The stacked MIM capacitor structure of claim 1, wherein a respective lower electrode of a respective MIM capacitor structure has a width dimension greater than a respective upper electrode.

24. (previously presented) The stacked MIM capacitor structure of claim 1, wherein an upper and lower electrode of an uppermost MIM capacitor structure respectively electrically communicate with respective overlying bonding pads.

25. (previously presented) The stacked MIM capacitor structure of claim 1, wherein said electrically communicating vias comprise vias extending through said first and second IMD layers.

26. (previously presented) A stacked integrated circuit (IC) MIM capacitor structure comprising:

a first MIM capacitor structure disposed in a first IMD layer comprising a first upper electrode and a first lower electrode; and,

a second MIM capacitor structure arranged in stacked relationship in an overlying IMD layer comprising a second upper electrode and second lower electrode separate from said first upper and first lower electrode;

wherein, the first lower electrode is arranged in common electrical signal communication comprising electrically communicating vias with the second upper electrode and the first upper electrode is arranged in common electrical signal communication with the second lower electrode; and,

at least one additional MIM capacitor structure arranged in stacked relationship with respect to the second MIM capacitor structure to form an MIM capacitor stack wherein respective upper and lower electrodes of respective odd and even numbered MIM capacitor structures in the MIM capacitor stack comprise a commonly communicating electrical

interconnect structure in parallel electrical relationship.

27. (previously presented) The stacked MIM capacitor structure of claim 26, further comprising a first and second uppermost conductive portion disposed overlying an uppermost IMD layer disposed to respectively provide electrical signal communication to said respective commonly communicating electrical interconnect structures.

28. (previously presented) The stacked MIM capacitor structure of claim 26, wherein the lower electrodes including electrically communicating vias of the respective MIM structures in the MIM capacitor stack comprise a substantially identical structure in alternating IMD layers.

29. (previously presented) A stacked integrated circuit (IC) MIM capacitor structure comprising:

a first MIM capacitor structure disposed in a first IMD layer comprising a first upper electrode and a first lower electrode; and,

a least a second MIM capacitor structure arranged in stacked relationship in an overlying IMD layer comprising a second upper electrode and second lower electrode separate from said first upper and first lower electrode to form an MIM capacitor stack;

wherein, the first lower electrode is arranged in common electrical signal communication

comprising electrically communicating vias with the second upper electrode and the first upper electrode is arranged in common electrical signal communication with the second lower electrode; and,

wherein the lower electrodes including electrically communicating vias of the respective MIM structures in the MIM capacitor stack comprise a substantially identical structure in alternating IMD layers.

30. (previously presented) The stacked MIM capacitor structure of claim 29, wherein respective upper and lower electrodes in said alternating IMD layers comprise a commonly communicating electrical interconnect structure in parallel electrical relationship.

31. (previously presented) The stacked MIM capacitor structure of claim 30, further comprising a first and second uppermost conductive portion disposed overlying an uppermost IMD layer to respectively provide electrical signal communication to said respective commonly communicating electrical interconnect structures.